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DEVELOPMENT OF HIGH PERFORMANCE ELECTRONICS AND OPTICAL-TO-ELECTRICAL ADVANCED CIRCUITRY FOR PHOTONIC ANALOG-TO-DIGITAL CONVERTERS

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Mayo has collaborated with AFRL on the study of an optical to electrical architecture for a high performance photonic-based analog-to-digital converter. This document summarizes the work comprising this study and the resulting conclusions.

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1 Introduction

Electronic ADCs use electrical signals to quantize and sample analog signals to convert them to digital signals. State-of-the-art commercially available electronic ADCs have aperture jitter on the order of 0.1 ps to 2 ps [1, 2]. This amount of aperture jitter, combined with comparator ambiguity, limit the resolution of electrical ADCs as the sampling frequency approaches 10 Gs/s. To achieve high resolution at 10 Gs/s sampling rates, the aperture jitter needs to be reduced to the order of 10 fs to 50 fs. Mode-locked lasers with low phase noise (50 fs) have been demonstrated and can be used for optical sampling systems, suggesting that ADCs utilizing optical sampling techniques might be produced which out-perform electronic ADCs.

The Air Force Research Laboratory/Rome (AFRL/Rome) has performed extensive research in photonics and anticipates that optical sampling can be used for the conversion of analog signals into digital signals at 10 Gs/s with extremely high resolution on the order of 12 to 14bits [4]. AFRL also anticipates that 100 Gs/s ADCs with multiple bits of resolution will be possible in the near future. While AFRL expertise in photonics is extensive, in order to prove out these ideas, AFRL sought expertise in the area of high speed electrical components which would be required to complete a photonic ADC system.

To this end, the Special Purpose Processor Development Group (SPPDG), Mayo Clinic, was contracted by AFRL to study potential architectures for the optical-to-electrical (O/E) conversion stage of high-performance (10 Gs/s to 100 Gs/s) photonic analog-to-digital converters (ADCs). In the original statement of work [3], Mayo proposed six tasks starting with the O/E architecture study in TASK 1 and ending with an integrated “near monolithic” photonic ADC in TASK 6. A budget for all six tasks was also proposed. Due to funding circumstances at AFRL, it was decided that Mayo would work on TASK 1 and write a report summarizing the O/E architecture study. This paper serves as the final report for this study.

2 Architecture Overview

For this O/E architecture study, AFRL has proposed a novel photonic ADC architecture that quantizes and samples the analog signal optically versus electrically [4, 5]. There are two main advantages of optical sampling employed in this architecture. First, the sampling clock is generated optically with a mode-locked laser which results in a low-jitter clock. Second, the analog signal is quantized optically, which simplifies the complexity of the electrical portion of the photonic ADC.

A block diagram illustrating the proposed optical and electrical sections of a 3-bit photonic ADC is shown below in Figure 1. The optical section was designed by AFRL and the electrical section was designed by Mayo as a result of this O/E architecture study. The operation of the optical section will be discussed first followed by the details of the electrical section.

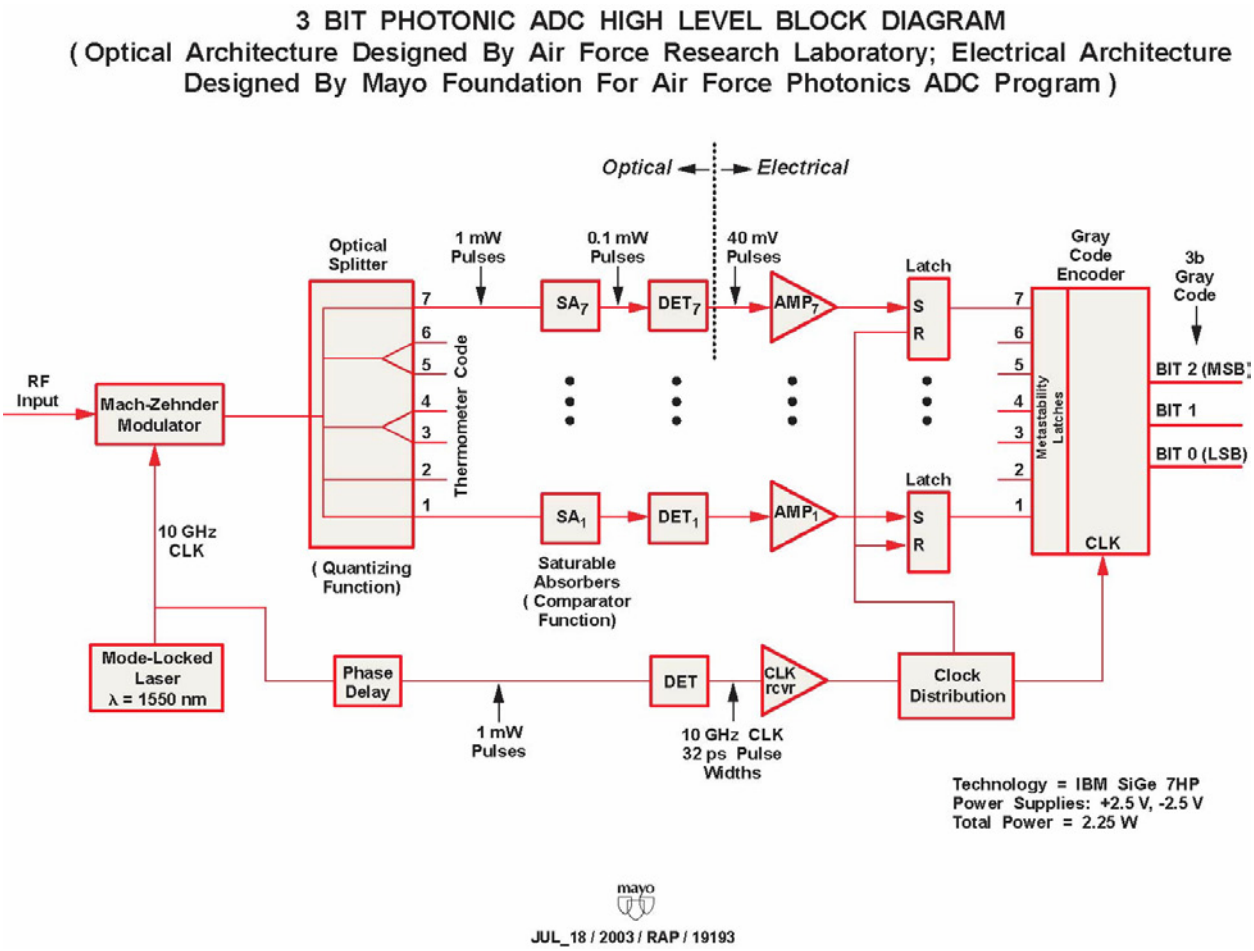

Figure 1: Photonic ADC Block Diagram (19193)

2.1 Optical Section Overview

The mode-locked laser generates the main clock for the optical and electrical sections of the photonic ADC. The wavelength of the laser is 1550 nm. The output of the laser is a continuous series of light pulses with a period of 100 ps. AFRL measured the full width half max duration of the light pulses from their mode-locked laser at 14.82 ps. These numbers translate to a sampling clock with a duty cycle of approximately 15%. The laser output is optically split into two fibers. One fiber is connected to a Mach-Zehnder modulator and the other is phase delayed and used to clock the electrical section of the ADC. The radio frequency (RF) input signal is connected to the electrical input of the Mach-Zehnder modulator. The electrical input signal modulates the intensity of the light pulses from the mode-locked laser, thereby capturing a sample of the RF input signal encoded in the intensity of each optical pulse

and performing the ADC sampling function. The modulated light pulses from the Mach-Zehnder modulator are optically connected to an optical splitter.

The optical splitter performs the quantizing function for the photonic ADC. For the 3-bit system illustrated in Figure 1, the optical splitter has seven optical outputs. The relative amplitudes of these seven optical outputs are weighted such that, after quantization, they collectively represent a thermometer code representation of the RF input signal amplitude. The seven optical splitter outputs are connected to seven saturable absorbers (SA1 – SA7). The saturable absorbers function as the comparators for the photonic ADC. Each saturable absorber has a 1 mW power threshold. No light passes through the saturable absorber when the incident light power is below 1 mW. Once the incident light power is above 1 mW the saturable absorber transmits light with a power of 0.1 mW. The output of each saturable absorber is connected to a photodiode. The photodiode converts the optical power to electrical current. It is at this point where the optical to electrical conversion takes place. Before the electrical section of the photonic ADC is discussed, the performance of the photodiodes will be summarized.

2.2 Photodiode Performance

For this architecture study, AFRL and Mayo elected to use Discovery Semiconductors, Inc., DSC-30S, Wide Bandwidth High Power Low Distortion PIN Diode [6, 7]. AFRL characterized the DSC-30S with 0.117 mW of input power pulses that would be representative of the light pulses output from the saturable absorbers. The output of the DSC-30S generated a 40 mV pulse with a full width half max value of 32 ps when terminated into 50 ohms. This data played a key role in directing the electrical architecture. The electrical pulse from the DSC-30S PIN diode was large enough that it could be amplified and then captured with an asynchronous current mode logic (CML) latch.

Before the DSC-30S PIN diode was characterized it was believed that the current pulses from the PIN diode would be so small that they would have to be integrated onto a capacitor and sampled. This would require sample and hold and reset circuitry which can add sampling noise and reset errors on the integrating capacitor. Correlated double sampling (CDS) is commonly used to cancel the many errors associated with sampling and resetting an integration capacitor [8, 9]. Fortunately for this architecture study, the performance of the DSC-30S PIN diode didn't

require an integration capacitor. The signal from the diode could be directly amplified with a high-bandwidth, low-gain amplifier.

To model the DSC-30S, a pulsed current source was used to drive a parallel combination of a 50 ohm resistor and a 250 fF capacitor to ground. Simulation models were created to represent the loading of the test equipment used by AFRL for the DSC-30S characterization. Once the simulation models were complete, the parameters of the pulsed current source were adjusted to reproduce the measured waveform of the DSC-30S.

2.3 Electrical Section Overview

The electrical section of the photonic ADC, shown above in Figure 1, begins with the amplifiers (AMP1 – AMP7) that amplify the 40 mV pulses from the PIN diodes (DET1 – DET7). The amplifiers convert the single-ended 40 mV signals from the PIN diodes to differential signals with amplitude of 250 mV to 300 mV. The differential signal from each amplifier is connected to the "Set" input of an asynchronous Set-Reset (SR) latch.

The outputs of the SR latches are synchronized to the system clock with seven metastability latches. The metastability latches are clocked by a delayed copy of the optical sampling clock that is converted to an electrical clock by the clock-receiver (CLK rcvr). The clock-receiver creates a differential clock signal that is connected to a clock-distribution block. The clock-distribution block generates two phases of the clock. One phase is used to clock the metastability latches to capture the asynchronous data from the SR latches. The other phase is connected to the "Reset" inputs of the SR latches to reset them before the next set of pulses is expected from the amplifiers (AMP1 – AMP7).

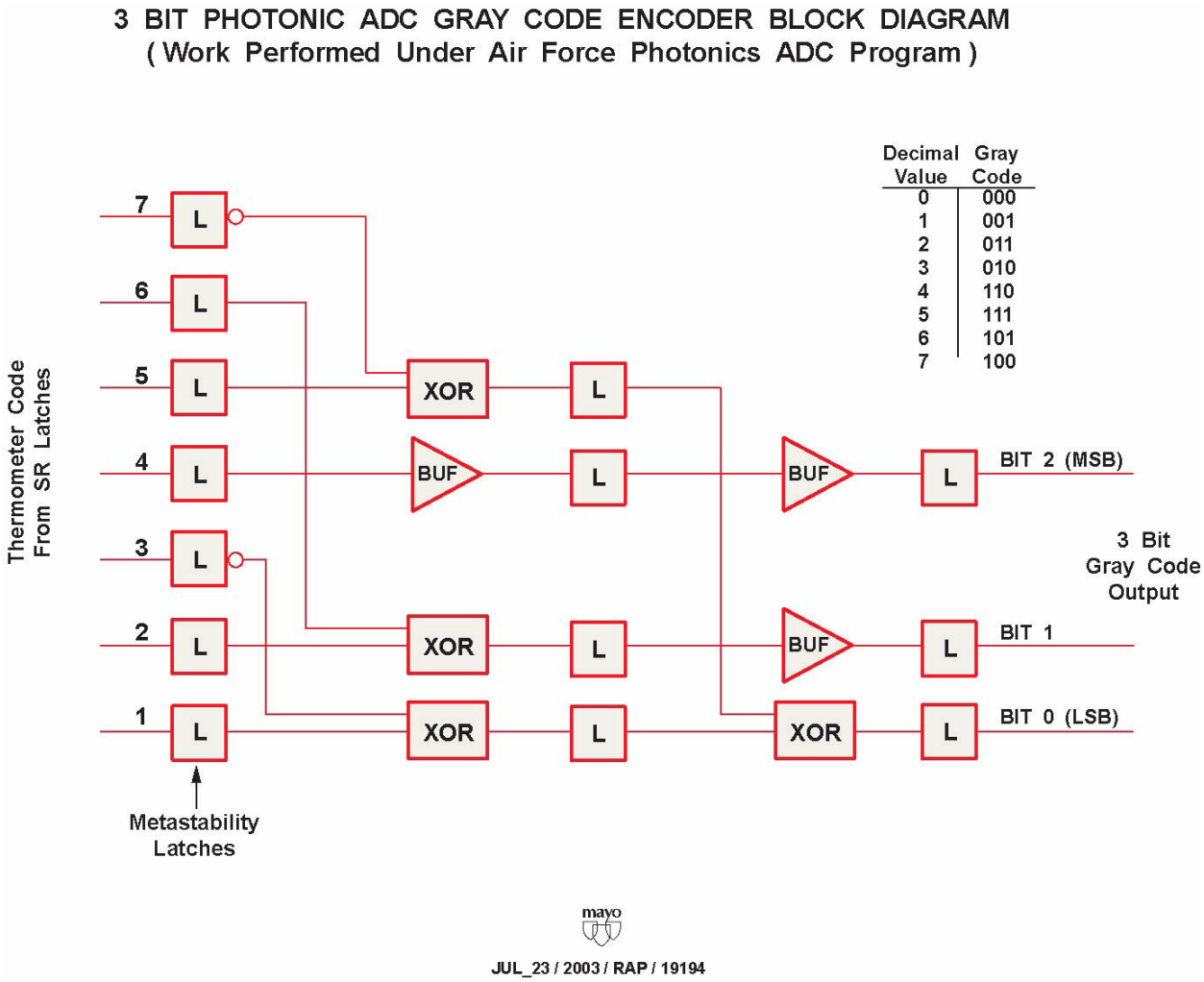

Figure 2: 3-Bit Photonic ADC Gray Code Encoder Block Diagram (19194)

Once the data has been captured by the metastability latches it is converted to a 3-bit Gray code. A detailed block diagram of the gray code encoder is shown above in Figure 2. The 3-bit Gray code encoder can be easily implemented with four exclusive (XOR) gates. In Figure 2, three buffers (BUF) were added along with additional latches. The buffers are needed to match the path delays between latches. The extra latches are needed to keep the data synchronized after each level of logic gates. The latches are clocked at 10 GHz which allows a 100 ps window for data to be processed by one level of logic (XOR's and BUF) before it is resynchronized by another set of latches.

Mayo implemented a 4-bit Gray code encoder in a different project with an expected performance of 20 GHz. Because of this experience, Mayo did not deem it necessary to re-simulate the 3-bit Gray code encoder logic used in this architecture study. Therefore the simulation model for the electrical section of the photonic ADC, shown above in Figure 1, stopped at the output of the metastability latches. The next section will discuss the circuit topologies for the amplifier, SR latch, clock receiver, clock distribution, and the metastability latch that were custom designed by Mayo for this O/E architecture study.

3 Circuit Details

Five key circuits needed to be designed for this architecture study. First, the amplifier used to amplify the single-ended 40 mV pulses from the photodiodes. Second, the SR latch needed to asynchronously capture the data pulses from the amplifiers. Third, the clock receiver which was modified version of the amplifier. Fourth, the clock distribution circuitry for the SR latches and metastability latches. Fifth, the metastability latches used to synchronize the data from the SR latches. Mayo used IBM's SiGe BiCMOS 7HP technology with Ft and Fmax of 120 GHz and 100 GHz respectively for circuit design and simulations [10]. The technology and the circuit topologies explored led to the use of positive and negative 2.5 V power supplies. Additional comments about technology options will be discussed in the conclusions section of this report.

3.1 Amplifier

Shown below in Figure 3, is a detailed block diagram of the amplifier (AMP) used in one of the seven thermometer code data paths. Each amplifier has a signal input pin (INP) and a reference input pin (REF). Both inputs are 50 ohm terminated to ground. The signal input pin is connected to an external pad that would be connected to the output of the DSC-30S PIN diode. The reference input is connected to an adjustable bias reference that is used to set the threshold voltage for the amplifier. The programmability of the threshold voltage allows the amplifier circuit to be used with other PIN photo-detector diodes with different output voltages as they

become available. In Figure 3, the bias reference is controlled with an external analog voltage. Other options would be to control the bias reference circuit with a digital-to-analog converter (DAC). In this study the threshold voltage was set to 12 – 15 mV for simulations.

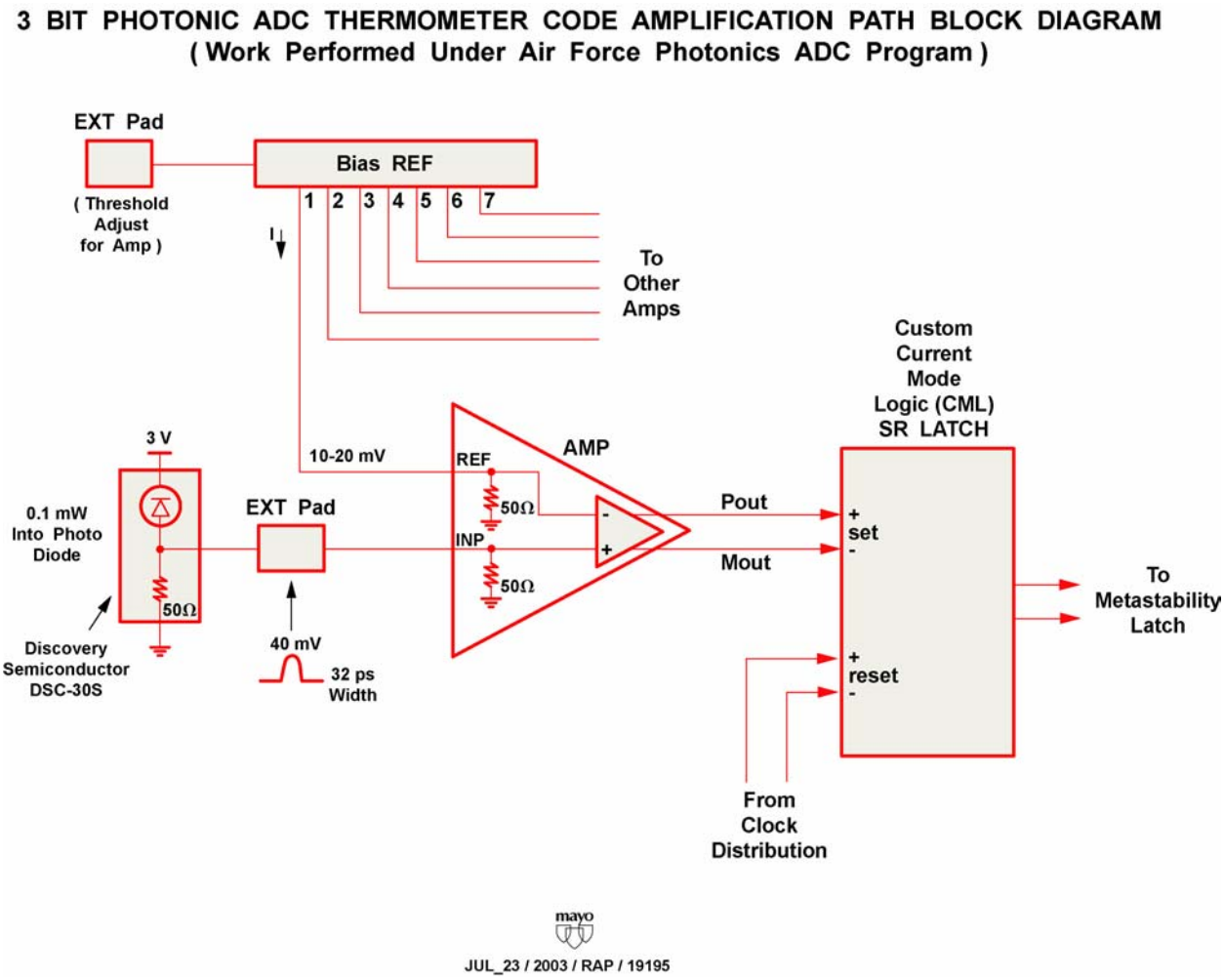

Figure 3: Thermometer Code Amplification Path Block Diagram (19195)

The output of the amplifier is differential with amplitude swings of 250 mV to 300 mV. These differential outputs can also be referred to as current mode logic (CML) levels. Each amplifier output is connected to the "Set" input of a CML SR latch. The SR latch is used to capture the asynchronous amplified pulsed data from the PIN diode. The output of the SR latch

is then synchronized to the system clock by the metastability latches. The schematic of the amplifier will be discussed next followed by the SR latch in the next section.

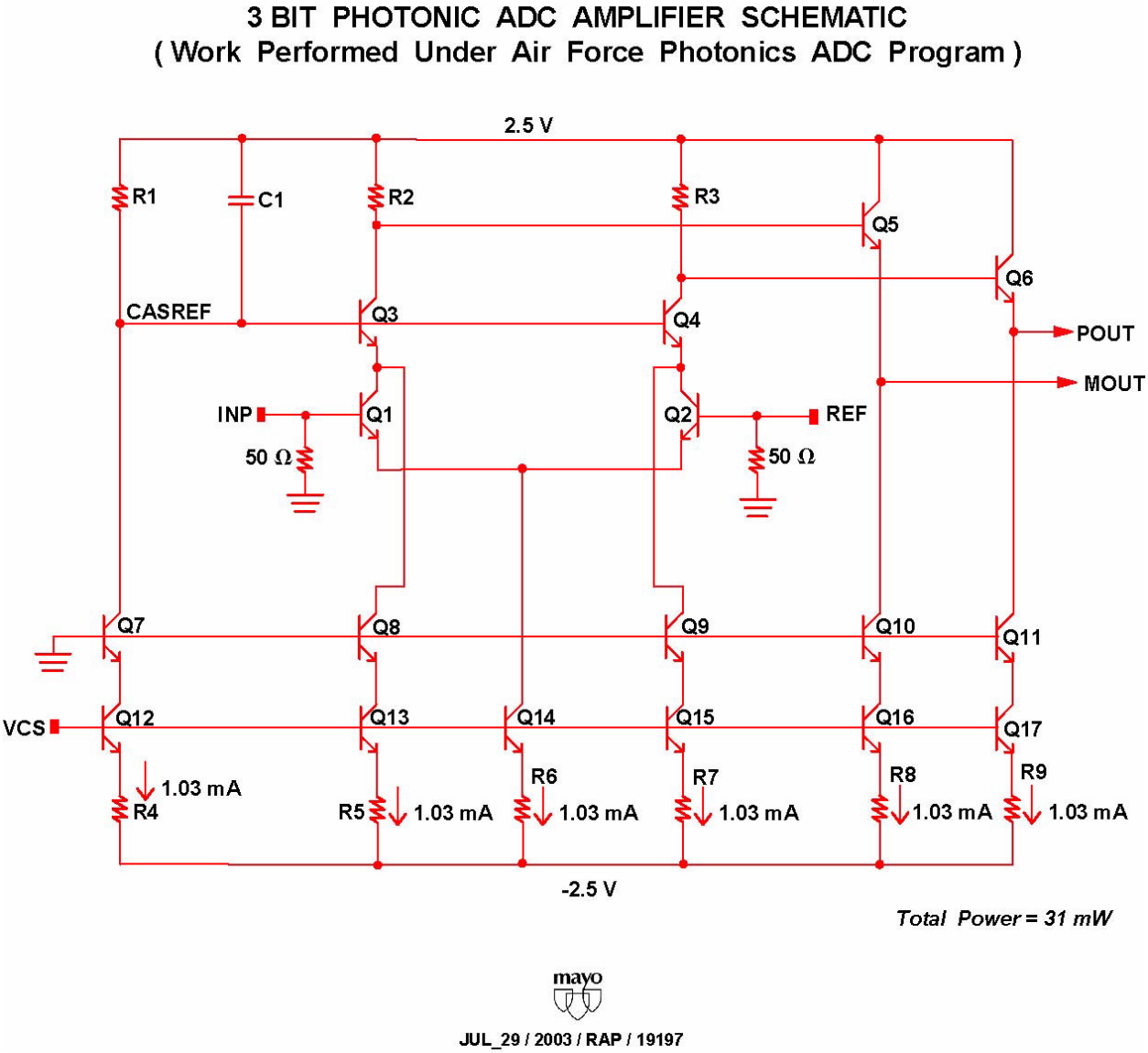

Figure 4: Amplifier Schematic (19197)

The schematic for the amplifier is shown above in Figure 4. Input pins INP and REF both have 50 ohm termination resistors to ground. The main input differential pair is transistors Q1 and Q2. The outputs of Q1 and Q2 are cascoded by transistors Q3 and Q4. Q3 and Q4 improve the bandwidth of the main input differential pair by reducing Miller capacitance

coupling from the collector to the base for Q1 and Q2 by holding the collectors of Q1 and Q2 at a relatively constant voltage. Additional bandwidth and improved pulse response was achieved by the addition of extra bias currents pulled from the emitters of cascode transistors Q3 and Q4. This was a key enhancement to improve the amplifier's transient pulse-response characteristics and minimize distortion of the 32 ps pulses from the DSC-30C PIN photo-detector diodes.

The gain of the amplifier is set by the input differential pair Q1 and Q2 and the collector resistors R2 and R3. The output nodes of resistors R2 and R3 are buffered and level shifted by emitter-follower transistors Q5 and Q6. The output pins POUT and MOUT connect directly to the "Set" input of the SR latch.

A separate circuit, not illustrated in this report, is used to generate the VCS bias voltage for the current sources located along the bottom of Figure 4. The main cascode transistors Q3 and Q4 have their bias reference voltage (CASREF) set by resistor R1. Capacitor C1 is used to filter off any noise on CASREF.

3.2 SR Latch

The schematic for the SR latch is shown below in Figure 5. There are two sections to this circuit. The left section is used to convert the high speed CML signals on the set (+Set, -Set) and reset (+RST, -RST) pins to controlled single-ended voltage swings. The right section of this circuit is the main SR latch. The boundary between the two sections is defined by drawing an imaginary vertical line between transistors Q9 and QSET. Each section will be discussed in detail next.

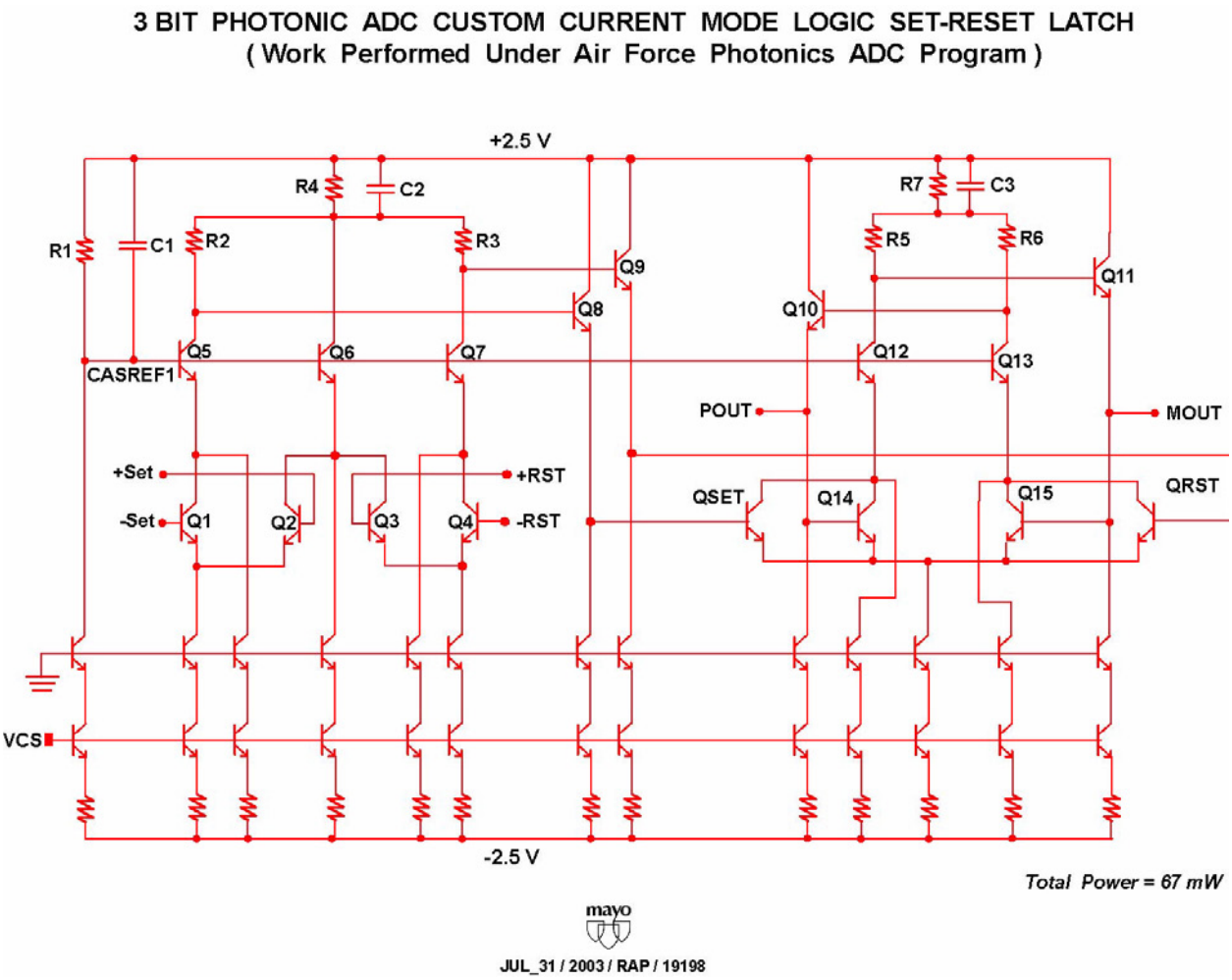

Figure 5: Current Mode Logic (CML) SR Latch (19198)

Transistors Q1 and Q2 form a differential pair for the set inputs (+Set, -Set). Transistors Q3 and Q4 form a differential pair for the reset inputs (+RST, -RST). The outputs of these differential pairs are connected to cascode transistors Q5 - Q7. Note that transistors Q2 and Q3 share the same cascode transistor Q6. The purpose for this will be discussed later. The bias reference voltage (CASREF1) is set by resistor R1 and is filtered by capacitor C1. Cascode devices Q5 - Q7 all have an additional bias current pulled from their emitters to improve bandwidth and transient pulse response. The outputs of cascode transistors Q5 and Q7 are connected to resistors R2 and R3 respectively. The output of cascode transistor Q6 is connected to resistor R4. R4 is used to set the positive voltage swing reference for resistors R2 and R3. Capacitor C2 is used to filter the positive swing reference set by resistor R4. The voltage swings

across resistors R2 and R3 are buffered and level shifted by emitter-follower transistors Q8 and Q9 respectively. The outputs of Q8 and Q9 drive the master set and reset transistors QSET and QRST respectively of the SR latch.

The SR latch is defined by transistors QSET, QRST, Q10 - Q15, resistors R5 - R7 and capacitor C3. The internal voltage swings for the SR latch are set by resistors R5 and R6. Resistor R7 defines the positive voltage swing for resistors R5 and R6. Transistors Q10 and Q11 are emitter-followers that provide the internal feedback for the SR latch to hold its state once it has been set or reset. Q10 and Q11 also drive output pins POUT and MOUT.

The transistors and resistors located along the bottom one-third of the schematic in Figure 5 are cascoded current sources that provide bias currents for the circuitry above. The reference voltage for the current sources is pin VCS. The reference voltage for the cascode transistors is the ground pin. The current sources are cascoded for two reasons. First, the output impedance of the current sources is increased by a minimum factor of 10. This improves power supply rejection for the entire circuit. Second, the cascode devices reduce the amount of voltage applied to the outputs of the current source transistors. This is very important for SiGe transistors which have a low breakdown voltage in the range of 1.55 V to 2.0 V [10].

3.3 Clocking Receiver and Distribution

The clock for the electrical section of the photonic ADC is a delayed version of the optical sampling clock as shown in Figure 1. The delayed optical clock is directly connected to a DSC-30S PIN photodiode without a saturable absorber present. This allows 1 mW of power to be received by the photodiode. AFRL characterized the DSC-30S with 1.0 mW and 1.3 mW of incident power. The results were output voltage pulses with amplitudes of 250 mV to 370 mV respectively and a full width half max value of 34 – 38 ps. A new model for the DSC-30S with larger input power was created using the same technique as described above in section 5.2 Photodiode Performance. The parameters of the current source were adjusted to generate a 370 mV pulse into a 50 ohm load with a pulse width of 34 ps.

The clock-receiver path is illustrated below in Figure 6. The clock-receiver has a similar circuit topology as the amplifier used in each thermometer code data path as illustrated above in Figure 4. The clock-receiver was modified to accept larger input signals and drive the larger loads associated with the clock-distribution circuitry.

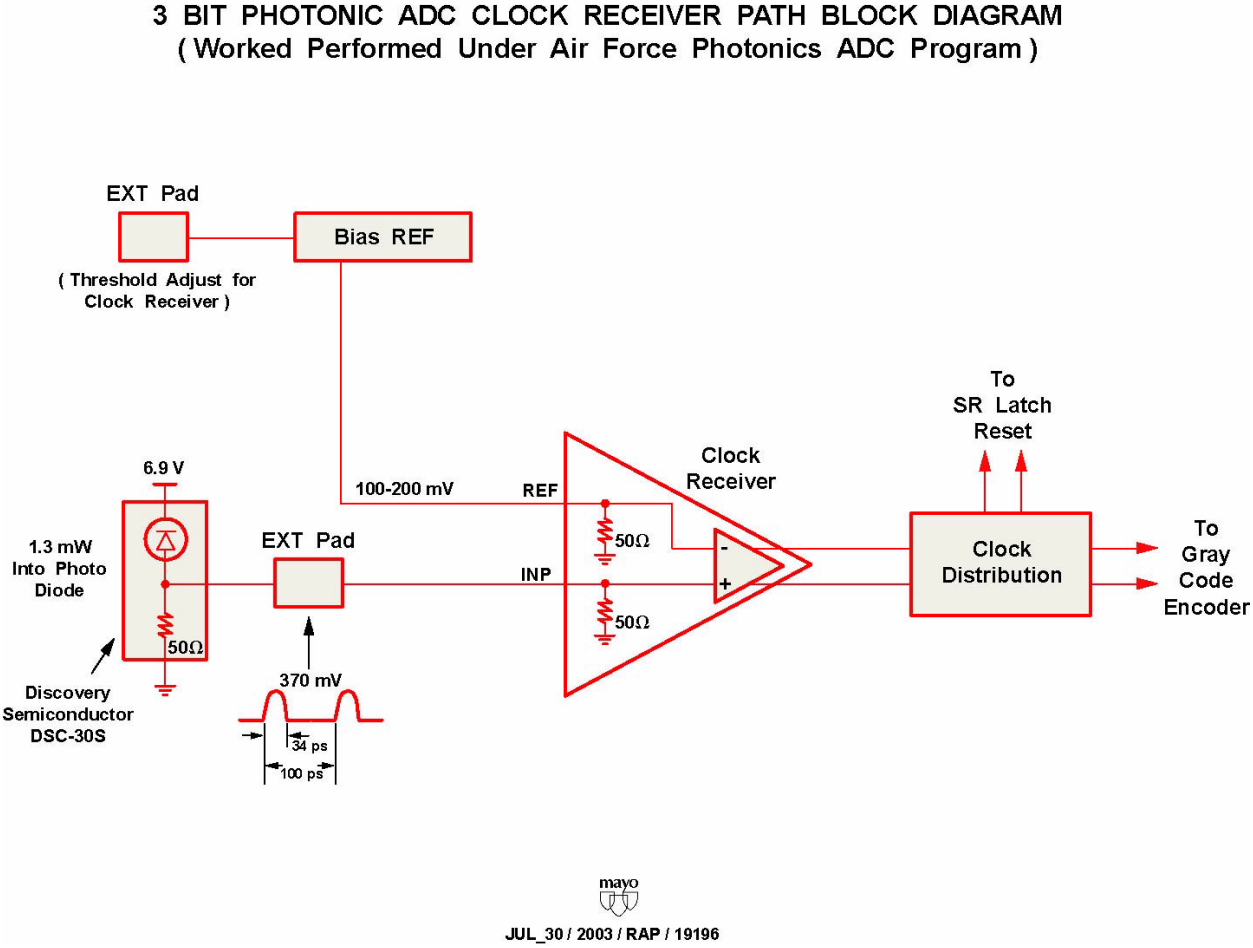

Figure 6: Clock Receiver Path Block Diagram (19196)

The clock-distribution circuitry consists of several CML high-power buffer circuits, pre-drivers, and drivers to fan out the clocks. The pre-drivers and drivers were used to drive the loads of the metastability latches. The buffers were used to delay the clock signal that reset the SR latches. The power consumed by the clock-distribution circuitry was approximately equal to the rest of the electrical section in the photonic ADC. Details on power consumption will be

discussed below in section 7.2. Very little time was spent optimizing the clock-distribution scheme due to funding constraints. This author believes that the clock-distribution power consumption could be reduced with additional design time and/or using higher Ft/Fmax transistors. Technology recommendations will be covered in section 8.

3.4 Metastability Latches

The metastability latches were implemented using a custom designed D-latch. The schematic for the custom latch is shown below in Figure 7. The circuit topology for this D-latch was originally designed at Mayo for a different program and is currently being evaluated in hardware. The custom latch was modified for the photonic ADC study to be compatible with the data signal levels from the SR latches. The unique feature of this D-latch is that the clock signals are driven at the top level of transistors (Q3 - Q10), while the data inputs are shifted down one level and driven into transistors (Q1 and Q2). This is just the opposite compared to a typical CML D-latch that has the data inputs driven at the top level and the clock inputs shifted down one level. Transistors (Q11 and Q12) are emitter-followers that drive output pins (MOUT and POUT) and provide internal feedback within the latch to hold previous data state on transistors (Q13 and Q14).

The motivation to create this custom latch was twofold. First, the clocking was moved to the top-level transistors (Q3 - Q10) to improve performance and minimize the amount of clock noise present on the output. Clock noise on the data output is minimized due to transistors (Q4 and Q5) and (Q8 and Q9) which are connected to opposite phases of the clock. Thus the base to collector feed through from CLKP on Q4 and Q5 is simultaneously cancelled by CLKM on Q8 and Q9. Second, with the data inputs level shifted down one level this latch can easily be modified to integrate logical operators (e.g. XOR) into the front-end. This technique has been done at Mayo under a different program and is currently being evaluated in hardware. These latches could also be used to implement the 3-bit Gray code encoder shown above in Figure 2.

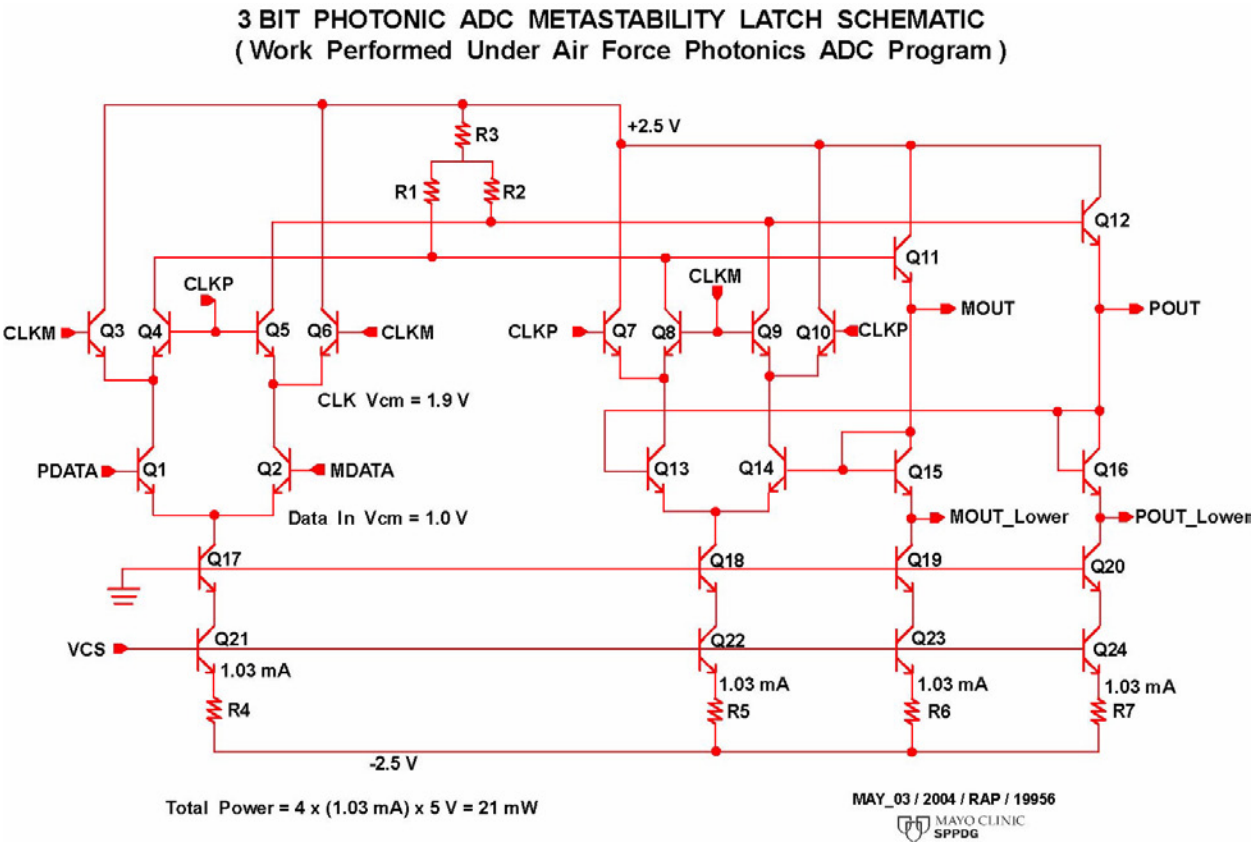

Figure 7: Custom Metastability D-Latch (19956)

4 Top Level Simulations and Results

A complete simulation model of the 3-bit photonic ADC shown in Figure 1 was assembled and simulated. The simulation model included the Mayo generated models for the DSC-30S photodiodes, amplifiers, SR latches, metastability latches, clock receiver, and clock distribution buffers. The XORs, buffers, and latches in the gray code encoder show in Figure 2 were not included. Simulations were run using +2.5 V and -2.5 V power supplies and a system clock of 10 GHz. Various data patterns were input into amplifiers from the photodiodes to verify the correct functionality of the SR latches and metastability latches.

4.1 Timing Diagram

Figure 8 below, contains simulation results for thermometer-code paths 1 and 2. The waveforms originated as differential signals but have been converted to single-ended waveforms to simplify the presentation. Each waveform is labeled along the right side of the figure. The top line is a series of numbers labeled “Input Amplitude”. These numbers represent the decimal value of the input amplitude applied to the ADC in terms of thermometer code. The first two values are “0” which results in an input amplitude below the threshold of saturable absorber (SA1). No data pulses were amplified by AMP1 (Amp Out 1) or AMP2 (Amp Out 2) and SR latches (1 and 2) were not set.

The next data pattern was “1 0”. This results in an isolated pulse from AMP1 that is used to set SR latch 1 for one clock period. Metastability latch 1 captures the data from SR latch 1 before SR latch 1 is reset by the SR Reset Signal. The clock signal for the metastability latches is the top waveform (Buffered CLK). The SR latch reset signal (SR Reset Signal) is located at the bottom of the page. It is hard to see, but the SR latch reset signal is a delayed version of the metastability (Buffered CLK) signal. This allows the metastability latches time to capture the data from the SR latches before they are reset. The clock (Buffered CLK) for the metastability latches has a much bigger load on it compared to the SR latch reset signal. The result is a rounded off clock waveform for Buffered CLK. Additional design time could be used to increase the drive of the clock-distribution circuitry and/or reduce the loading of the metastability latches.

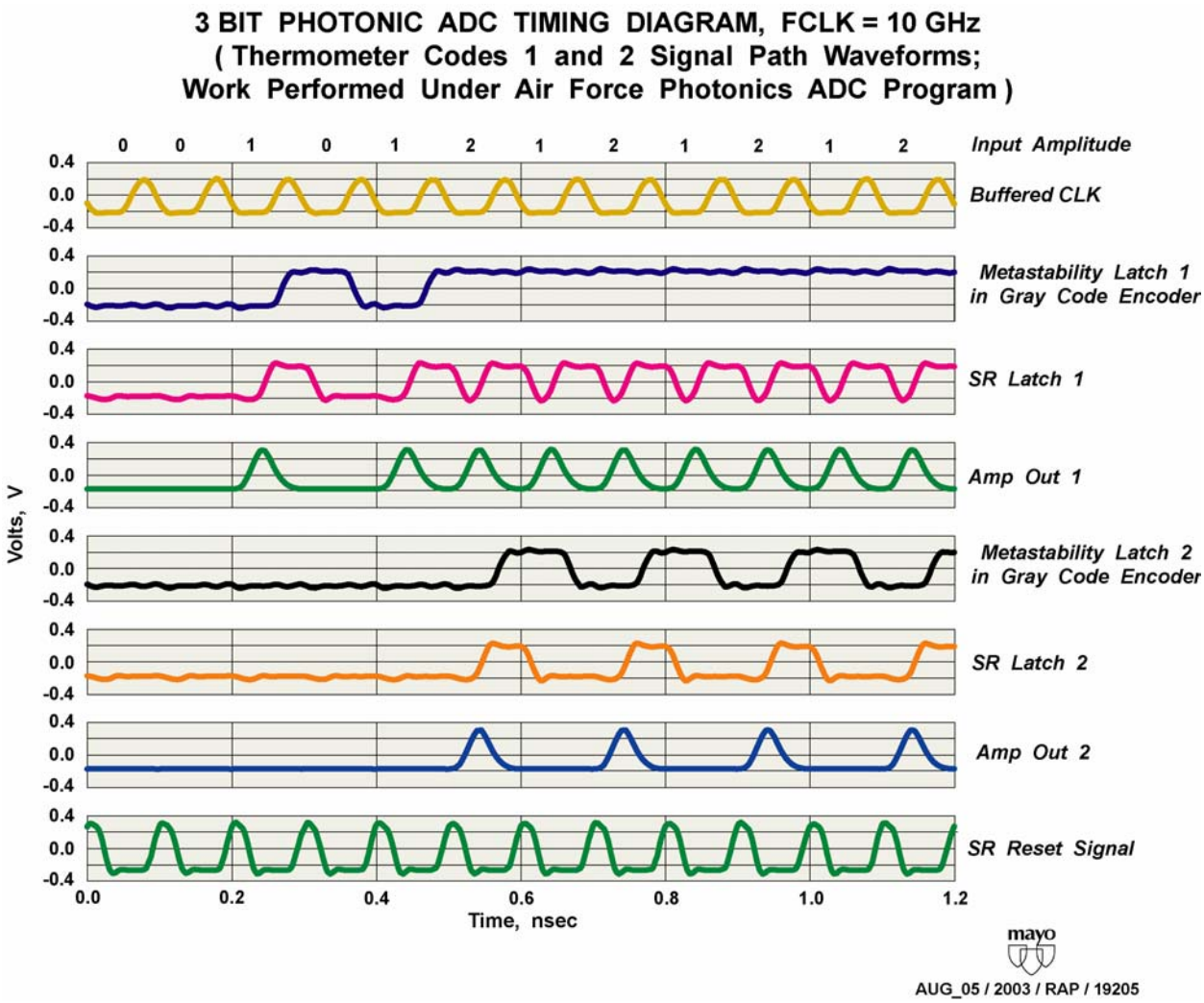

Figure 8: 3-Bit Photonic ADC Timing Diagram (19205)

The remaining data patterns are decimal values 1 and 2, which show the effects of when both amplifiers (Amp Out 1 and 2) send pulses to SR Latches 1 and 2. Data is then captured by Metastability Latches 1 and 2. Since the value is always equal to or greater than 1 it can be observed that AMP 1 always sends a pulse to set SR Latch 1 every period. SR Latch 1 is always high when Metastability Latch 1 samples it resulting in the output of Metastability Latch 1 remaining high every clock period. This is a feature that minimizes the number of transitions each metastability latch has to make. Thus the maximum data switching rate for any metastability latch is every other clock period. This effect can be observed in Figure 8 looking at the waveform labeled "Metastability Latch 2 in Gray Code Encoder."

4.2 Power Consumption

The power consumption for the 3-bit photonic ADC is presented in the following three tables. The tables illustrate the amount of power that is needed for ADC function (Table 1) versus the clock distribution circuitry (Table 2). The power numbers were obtained from simulations using nominal power supplies (+2.5 V and -2.5 V) and nominal temperature (25 C). Since the 3-bit Gray code encoder and off chip drivers were not simulated as part this study, the power for these circuits is estimated and is prefixed with an asterisk. Table 3 shows the total power for the electrical section of 3-bit photonic ADC proposed in this study.

Circuit	Circuit Power	Quantity Needed	Total Power
Amplifier	31mW	7	217mW
SR Latch	67mW	7	469mW
Metastability Latches	21mW	7	147mW
Bias References	6mW	7	42mW
* Encoder Latches with Integrated Logic	21mW	7	147mW
* Bias Reference for Encoder	6mW	2	12mW
* Off Chip 50ohm Drivers	40mW	3	120mW
Total Power for ADC Function			1154mW

Table 1: Power Required for ADC Function and Off Chip Drivers

Circuit	Circuit Power	Quantity Needed	Total Power
Clock Receiver	47mW	1	47mW
Clock Buffers	47mW	2	94mW
Pre Drivers	98mW	4	392mW
Clock Drivers	114mW	2	228mW
Bias References	6mW	4	24mW
* Encoder Pre Driver	98mW	1	98mW
* Encoder Clock Driver	189mW	1	189mW
* Encoder Bias References	6mW	4	24mW
Total Power for Clock Circuitry			1096mW

Table 2: Power Required for Clock Distribution Circuitry

Circuit	Power
ADC Function	1.154W
Clock Distribution	1.096W
Total Power for 3b Photonic ADC	2.25W

Table 3: Total Power for 3-bit Photonic ADC

5 Conclusions

The purpose of this final report was to document the results of Mayo's architecture study to support AFRL in the implementation of a 3-bit photonic ADC. Mayo architected the electrical section based on the system requirements from ARFL and the characterization data obtained by ARFL for the Discovery Semiconductor DSC-30S PIN photo-detector diode. The design and simulations were performed using IBM's SiGe BiCMOS 7HP technology with Ft and Fmax of 120 GHz and 100 GHz respectively, which was the state-of-the-art SiGe technology available

when this study was performed [10]. After the study concluded, IBM released its SiGe BiCMOS 8HP technology with Ft and Fmax of 205 GHz and 200 GHz respectively [11]. SiGe BiCMOS 8HP would result in a lower power design for two reasons. First, the higher Ft/Fmax transistors would require less bias current for the same performance, resulting in lower power consumption. Second, the power supply voltages could be reduced from +/- 2.5 V to +/-2.0 V or +/- 1.8 V, which would also reduce power consumption. Other technology recommendations would include Indium Phosphide (InP), which is known for its high-performance transistors. At the time of this writing, InP production transistors are available with Ft/Fmax of 300 – 350 GHz and state-of-the-art transistors with even higher Ft/Fmax. The author believes the power could be reduced from 2.25 W to 1.75 W to 1.5 W using either SiGe 8HP or InP.

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